WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an uppermost layer wiring formed on a semiconductor substrate;

a rewiring layer formed so as to be connected to said uppermost layer wiring through a protection film; and

a bump connected to said rewiring layer,

wherein said semiconductor device has at least one uppermost layer element wiring structure located below said bump and having the uppermost layer wiring with a larger area than a connecting area between said bump and said rewiring layer.

2. A semiconductor device according to claim 1, wherein said bump is formed within a region of a wiring width of said uppermost layer wiring.

3. A semiconductor device comprising:

an uppermost layer wiring formed on a semiconductor substrate;

a rewiring layer formed so as to be connected to said uppermost layer wiring through a protection film; and

a bump connected to said rewiring layer,

wherein said bump is formed outside above the edge of the uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump.

4. A semiconductor device according to claim 3, wherein said bump is formed outside above the edge of said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump.

5. A semiconductor device according to claim 3, wherein said bump is formed within a region of a wiring width of said uppermost layer wiring.

6. A method of designing a semiconductor device comprising an uppermost layer wiring connected to an element region formed on a semiconductor substrate, a rewiring layer formed so as to be connected to said uppermost layer wiring through a protection film and a bump connected to said rewiring layer, wherein a process of arranging said bump comprises steps of:

detecting whether or not an edge of said uppermost layer wiring exists within a region where said bump is to be arranged; and

arranging said bump so that it is located outside above the edge of said uppermost layer wiring.

7. A method of designing a semiconductor device according to claim 6, wherein in said step of detecting, if it is decided that the edge of said uppermost layer wiring exists within the region where said bump is to be arranged, said bump is formed to be located outside above the edge of said uppermost layer wiring, by adjusting

the size of said bump.

8. A method of designing a semiconductor device according to claim 6, wherein the size of said bump is made smaller than the wiring width of said uppermost layer wiring so that the bump is located within a region of said wiring width.

9. A method of designing a semiconductor device comprising an uppermost layer wiring formed on a semiconductor substrate, a rewiring layer formed through a protection film and a bump connected to said rewiring layer, wherein a process of arranging said bump comprises a step of:

arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to a different node from that of the rewiring layer connected to said bump.

10. A method of designing a semiconductor device according to claim 9, wherein the process of arranging said bump comprises a step of:

arranging said bump so that it is located outside above the edge of said uppermost layer wiring connected to the same node as that of the rewiring layer connected to said bump.

11. A method of designing a semiconductor device according to claim 9, wherein the process of arranging said bump

comprises a step of:

arranging said bump so that it is located within a region of a wiring width of said uppermost layer wiring.

12. A method of designing a semiconductor device according to claim 9, wherein the process of arranging said bump comprises a step of:

arranging said bump so that it is located outside a region where said uppermost layer wiring exists.

13. A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 1 is located beneath each of all bumps.

14. A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 2 is located beneath each of all bumps.

15. A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 3 is located beneath each of all bumps.

16. A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 4 is located beneath each of all bumps.

17. A method of designing a semiconductor device comprising a step of arranging the uppermost layer element wiring structure described in claim 5 is located beneath each of all bumps.